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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,741	12/29/2003	Takahisa Ueno	SON-4664/DIV	2068

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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/747,741	UENO ET AL.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17 and 24-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,24-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to newly added claims 24-33 filed on 02/24/2011 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments with respect to claim 17 filed on 02/24/2011 have been fully considered but they are not persuasive.

In re pages 8-9, Applicants argue that Gowda fails to specify FET 22 being either an enhancement type transistor or a depletion type transistor.

In response, regarding claim 17, Applicant recites limitation "wherein said transfer switch is an enhancement type transistor." The Examiner considers that Gowda et al. do disclose this feature. Gowda et al. discloses the pixel circuit of cell 30 employs FET 22 to perform both a charge transfer function and a pixel selection function (FET 22, figure 3B, column 4, lines 9-36). It should be noted that FET is an enhancement type transistor. See Sauer (US 5,134,488), column 4, lines 10-12.

Therefore, the rejection of claim 17 is maintained, and this office action is made FINAL.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection

is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 24 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 3 of U.S. Patent No. 7,116,365. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason.

Claim 24 of the instant application is anticipated by Patent Claims 1 and 3 in that Claims 1 and 3 of the Patent contains all the limitation of claim 24 of the instant application. Note that the feature "each of said reset switches is a depletion type transistor" as claimed in Patent Claim 1 reads on limitation "said reset switch is a depression type transistor" as claimed in Claim 24 of the instant application. Claim 24 of the instant application therefore is not patently distinct from the earlier patent claim and as such is unpatentable for obvious-type double patenting.

5. Claim 26 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 33 of copending Application No. 10/945,519 (Amendment filed on 04/29/2011) in view of van Santen (US 4,168,444).

Regarding claim 26 of the instant application, Copending Application Claim 33 discloses all the limitations of the claim 26 of the instant application, except for the limitation "said reset switch being a depression type transistor."

However, van Santen discloses an imaging device in which an n-channel deep-depletion field effect transistor 91 (i.e., depression type transistor) which acts as a reset switch (column 7, line 65 – column 8, line 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in the Copending Application Claim 33 by the teaching of van Santen in order to drain away an information-representative charge-packet after sensing so resets the initial positive potential (column 8, lines 1-4).

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 5,898,168) in view of Tanaka et al. (US 6,674,470) further in view of Hamasaki (US 5,187,583).

Regarding claim 17, Gowda et al. discloses a solid state imaging element (imager 20, figures 3A-3B) comprising:

a plurality of pixels (plurality of cells 30, figures 3A-3B) arranged in a matrix, each of which (cell 30; figures 3A-3B; column 4, lines 9+) has a photoelectric conversion element (photodiode 26, figure 3B, column 4, lines 9-20), a transfer switch (FET 22, figure 3B, column 4, lines 9-36) for transferring charge stored in said photoelectric conversion element, a charge store part (circuit node 25, figure 3B, column 4, lines 37-62) for storing charge transferred by said transfer switch, a reset switch (reset transistor 21, figure 3B, column 4, lines 20-62) for resetting said charge store part, and an amplifying element (FET 23, figure 3B, column 4, lines 9-36) for outputting a signal in accordance with a potential of said charge stored in said charge store part (figures 3A-3B, column 4, lines 9-62).

Gowda et al. fails to specifically disclose wherein a threshold voltage of said amplifying element is reduced in relation to remaining transistors of each pixel. However, Tanaka et al. teaches an image sensor, in which the amplifying transistor has a low threshold voltage, this indicates that the threshold voltage of the amplifying is reduced (column 16, lines 50-55); and noted that each unit cell (pixel) in Figure 7 includes other transistors such as reset transistor 96, read-out transistors 93a, 93b in addition to amplifying transistor 94; all these transistors are connected each other (i.e., relation to each other); this indicates that the threshold voltage of the amplifying 94 is reduced in relation to reset transistor 96, read-out transistors 93a, 93b (column 16, lines 30-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Gowda et al. by the teaching of Tanaka et al. in order to obtain a solid state imaging device which have a wide amplifying function (column 16, lines 50-52);

wherein said transfer switch is an enhancement type transistor (FET 22, figure 3B, column 4, lines 9-36).

Gowda et al. and Tanaka et al. fail to disclose wherein a diffusion region that is connected to a power source is laid out to be physically adjacent to the photoelectric conversion element in order to provide an overflow path. However, Hamasaki discloses a solid state imager which comprises a floating diffusion (FD) connected to power supply voltage VDD and is adjacent to a photodiode (figures 1-2, column 3, lines 8-19; column 5, line 58 – column 6, line 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Gowda et al. and Tanaka et al. by the teaching of Hamasaki in order to provide an overflow train (column 5, line 58 - column 6, line 8).

8. Claims 24-25, 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 5,898,168) in view of Hamasaki (US 5,187,583) further in view of van Santen (US 4,168,444).

Regarding claim 24, Gowda et al. discloses a solid state imaging element (imager 20, figures 3A-3B) comprising:

a transfer switch (FET 22, figure 3B, column 4, lines 9-36) having a source and an drain being a photodiode (photodiode 26, figure 3B, column 4, lines 9-20),

a reset switch (reset transistor 21, figure 3B, column 4, lines 20-62) having a source and and a drain;

Gowda et al. fails to disclose a floating diffusion region. However, Hamasaki discloses a solid state imager which comprises a floating diffusion (FD) connected to a source of reset transistor 3 (figures 1-2, column 3, lines 8-19; column 5, line 58 – column 6, line 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Gowda et al. by the teaching of Hamasaki in order to provide an overflow train (column 5, line 58 - column 6, line 8).

Gowda et al. and Hamasaki fail to disclose said reset switch being a depression type transistor. However, van Santen discloses an imaging device in which an n-channel deep-depletion field effect transistor 91 (i.e., depression type transistor) which acts as a reset switch (column 7, line 65 – column 8, line 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Gowda et al. and Hamasaki by the teaching of van Santen in order to drain away an information-representative charge-packet after sensing so resets the initial positive potential (column 8, lines 1-4).

Regarding claim 25, Gowda et al. discloses wherein a matrix has a row (n) of pixels and a row (n+l) of pixels, each unit pixel (n, m) in said row (n) of pixels including said transfer switch and said reset switch (Figures 2, 3A, 3B, 14).

Regarding claim 27, Gowda et al. discloses wherein said row (n) is selected while said row (n+ 1) is non-selected, said row (n+l) being selected while said row (n) is non-selected (column 4, lines 52-54).

Regarding claim 28, Hamasaki discloses an amplifying switch (MOSFET 4, figure 1, column 3, lines 8-35) having a gate electrically connected to said floating diffusion, a source electrically connected to a vertical signal line, and a drain electrically connected to a power source line.

Regarding claim 29, Hamasaki discloses wherein said amplifying switch is an enhancement type transistor (MOSFET 4, figure 1, column 3, lines 8-35).

Regarding claim 30, Gowda et al. discloses wherein said transfer switch is an enhancement type transistor (FET 22, figure 3B, column 4, lines 9-36).

Regarding claim 31, Gowda et al. discloses wherein said transfer switch has a gate electrically connected to a transfer line (FET 22, figure 3B, column 4, lines 9-36).

Regarding claim 32, Gowda et al. discloses wherein said reset switch has a gate electrically connected to a reset line (reset transistor 21, figure 3B, column 4, lines 20-36).

Regarding claim 33, Gowda et al. discloses wherein said photodiode is configured to photoelectrically convert incident light into a signal charge (photodiode 26, figure 3B, column 4, lines 9-62).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571)272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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05/06/11